Claims

What is claimed is:

1. A semiconductor integrated circuit comprising:

a memory cell having a port through which data is input to and output from a set of bit lines when a word line is driven;

a write/read circuit connected with the port via the set of bit lines for writing data to the memory cell and for reading data from the memory cell;

a read circuit connected with the port via the set of bit lines for reading data from the memory cell;

a CPU-system control circuit that controls the write/read circuit so that a data write or read operation based on at least one of a write request and a read request from a CPU is performed for a first period; and

a display-system control circuit that controls the read circuit so that data to be supplied to a display panel is read for a second period which does not overlap the first period.

2. A semiconductor integrated circuit according to Claim 1, wherein the CPU-system control circuit includes:

a first circuit that activates a write control signal based on a write request signal sent from the CPU; and

a second circuit that activates a read control signal based on a read request signal sent from the CPU, and

the display-system control circuit includes a third circuit that activates a display-data read control signal based on at least the write request signal and

read request signal sent from the CPU and a display-data read request signal sent from a timing generator circuit.

3. A semiconductor integrated circuit according to Claim 2, wherein the third circuit activates the display-data read control signal based on the display-data read request signal sent from the timing generator circuit when the write request signal and read request signal sent from the CPU are inactive and when the write control signal and read control signal generated by the CPU-system control circuit are inactive.

4. A semiconductor integrated circuit according to Claim 2, wherein the third circuit starts activation of the display-data read control signal based on the display-data read request signal sent from the timing generator circuit when the write request signal and read request signal sent from the CPU are inactive and when the write control signal and read control signal generated by the CPU-system control circuit are inactive; and activates the display-data read control signal when the write control signal and read control signal generated by the CPU-system control circuit are inactive.

5. A semiconductor integrated circuit according to Claim 2, wherein the third circuit starts activation of the display-data read control signal based on the display-data read request signal sent from the timing generator circuit for a period except for a period after completion of activation of the write request signal sent from the CPU until completion of activation of the write control signal generated by the CPU-system control circuit and a period after completion of activation of the

read request signal sent from the CPU until completion of activation of the read control signal generated by the CPU-system control circuit; and activates the display-data read control signal for a first period when the write control signal and read control signal generated by the CPU-system control circuit are inactive,

the first circuit starts activation of the write control signal when a second period longer than the first period has elapsed after completion of activation of the write request signal sent from the CPU, and

the second circuit starts activation of the read control signal when a third period longer than the first period has elapsed after completion of activation of the read request signal sent from the CPU.

6. A semiconductor integrated circuit comprising:

a memory cell array including a plurality of memory cells that store data;

a CPU-system control circuit that divides the memory cell array into a plurality of blocks for control so that data is written or read based on a write request or read request from a CPU; and

a display-system control circuit that divides the memory cell array into a plurality of blocks for control so that data to be supplied to a display panel is not read from a block where data is being written or read based on a request from the CPU, and that divides the memory cell array into a plurality of blocks for control so that data to be supplied to the display panel is read from a block where data is not being written or read based on a request from the CPU.

7. A semiconductor integrated circuit according to Claim 1, wherein the memory cell further comprises an SRAM memory cell.

8. A semiconductor integrated circuit according to Claim 6, wherein the memory cell further comprises an SRAM memory cell.